REMARKS/ARGUMENTS

Claims 1-12 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. patent number 6,407,963 to Sonoda et al., which is referred to hereafter referred to as "Sonoda." Regarding claim 1, as well as the other claims, the Examiner contends that all of the claims' limitations can be found in Sonoda.

As is well known, a claim rejection made under 35 U.S.C. §102(b) must be based on a showing that each and every limitation of a claim can be found in a single reference, however, the Examiner failed to identify exactly *where* each claim's limitations are found in the Sonoda reference. In fact, the undersigned representative of the applicant searched for but was unable to locate *where* in the Sonoda reference, each and every one of the limitations of claim 1 is disclosed. It therefore appears that the claim rejections were improper.

The Examiner cites almost two full columns of Sonoda, i.e., col. 3 line 10 through col. 4, line 65, as ostensibly teaching just the first limitation of claim 1, which is "storing data, which are applied from a memory controller, in a data input latch through a data buffer and aligning the stored data." However, the Examiner cites the *same* passage of Sonoda, i.e., col. 3, lines 10-63, as also teaching the last limitation of claim 1, namely "enabling the data input latch to receive new data after the data, which have been transmitted to the data input/output detection amplifier, are transmitted to a global input/output line."

With regard to the first and last limitations of claim 1, the applicant has searched the Sonoda reference for the first and last limitations of claim 1 and contends that these two limitations of claim 1 are not in Sonoda. Unless the Examiner can identify by

column and line number, exactly where each of the limitations of claim 1 can be found in the Sonoda reference, the rejection of claim 1 should be withdrawn.

The Examiner's rejections of the other independent claims are similarly improper.

Under the rules of practice set forth in 37 C.F.R. §1.104(c)(2), an examiner is required to identify the particular part of the reference upon which a patentability rejection is based, when a reference is complex. The Examiner cannot honestly contend that Sonoda is a simple reference. That the Sonoda reference is complex is in fact tacitly admitted by Examiner's identification of *two full columns* of Sonoda as ostensibly teaching where the first limitation of claim 1 is found.

Under the Rules of Practice set out in Title 37 of the Code of Federal Regulations, the Examiner has not properly rejected the claims because the Examiner has not identified *where* the Examiner found the limitations of the pending claims in Sonoda. It appears that the Examiner did not in fact find the pending claim limitations and has instead chosen to obfuscate the true relevance of Sonoda.

Notwithstanding the Examiner's improper rejection, the applicant has amended the independent claims to clarify that the data in the data latch is held for a time interval determined by the delay circuit shown in FIG. 4. Since Sonoda does not teach any sort of temporal delay, the further amendment of the independent claims is believed to avoid Sonoda.

Since the Applicant has distinguished the claims from the art cited by the Examiner, claims 1-12 are submitted to be in condition for allowance.

Respectfully submitted,

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